

What is claimed is:

1 1. A double corner rounding process for a partial
2 vertical cell, comprising:

3 providing a substrate comprising a memory cell array
4 region and a supporting region and having a
5 first mask layer thereon, wherein a deep trench
6 is formed in the first mask layer and the
7 substrate in the memory cell region, a
8 capacitor is formed in a lower portion of the
9 deep trench, a first insulating is formed in
10 the upper portion of the deep trench, and the
11 surface of the first insulating layer is lower
12 than that of the substrate;

13 filling a second mask layer in the deep trench,
14 wherein the surface of the second mask layer is
15 lower than that of the first mask layer;

16 forming a photoresist layer on the active areas of
17 the substrate, such that a first portion of the
18 substrate, covered by the photoresist layer,
19 and a second portion of the substrate, not
20 covered by the photoresist layer, are defined;

21 removing parts of the first mask layer not covered
22 by the photoresist layer and the second portion
23 of the substrate until the surface of the
24 second portion of the substrate is lower than
25 that of the first mask layer;

26 removing the photoresist layer and the second mask
27 layer;

28 removing the edge of the first mask layer until the
29 corner of the first portion of the substrate is
30 exposed;
31 performing a first rounding process on the corner of
32 the first portion of the substrate;
33 conformally forming a second insulating layer on the
34 first mask layer , the first insulating layer,
35 and the substrate;
36 forming an insulating plug on the second insulating
37 layer, such that the surface of the insulating
38 plug is substantially level with that of the
39 second insulating layer on the substrate;
40 removing the insulating plug, the second insulating
41 layer, and the first mask layer from the memory
42 cell array to expose the corner of the first
43 portion of the substrate;
44 performing a second rounding process on the corner
45 of the substrate in the memory cell array
46 region.

1 2. The method as claimed in claim 1, wherein the
2 first mask layer comprises stacked silicon oxide and
3 silicon nitride layers.

1 3. The method as claimed in claim 1, wherein the
2 second mask layer is an organic anti-reflection coating
3 layer.

1 4. The method as claimed in claim 3, wherein
2 removal of the edge of the first mask layer is performed
3 by anisotropic etching.

1 5. The method as claimed in claim 4, wherein an
2 etching solution comprising hydrogen fluoride (HF) and
3 ethylene glycol (EG) is employed in anisotropic etching.

1 6. The method as claimed in claim 1, wherein the
2 first rounding process comprises oxidizing the corner and
3 the sidewall of the first portion of the substrate to
4 form a sacrificial oxide layer and removing the
5 sacrificed oxide layer.

1 7. The method as claimed in claim 6, wherein
2 oxidization is performed by in-situ steam generation
3 (ISSG).

1 8. The method as claimed in claim 1, wherein the
2 second insulating layer comprises silicon nitride.

1 9. The method as claimed in claim 1, wherein the
2 insulating plug comprises silicon oxide formed by high
3 density plasma chemical vapor deposition (HDP CVD).

1 10. The method as claimed in claim 8, wherein the
2 second rounding process is performed by employing an
3 oxidation agent and a HF solution by turns.

1 11. The method as claimed in claim 10, wherein the
2 oxidation agent comprises $\text{H}_2\text{O}_2(\text{aq})$ and $\text{HNO}_3(\text{aq})$.

1 12. The method as claimed in claim 1, further
2 comprising forming transistors on the active area in the
3 memory cell array region and in the supporting region.

1 13. A double corner rounding process for a partial
2 vertical cell, comprising:

3 providing a substrate comprising a memory cell array
4 region and a supporting region and having a
5 first mask layer thereon, wherein a deep trench
6 is formed in the first mask layer and the
7 substrate in the memory cell region, a
8 capacitor is formed in a lower portion of the
9 deep trench, a first insulating is formed in
10 the upper portion of the deep trench, the
11 surface of the first insulating layer is lower
12 than that of the substrate, and a shallow
13 trench is formed to define active areas in the
14 memory cell array region and the supporting
15 region;

16 removing the edge of the first mask layer until the
17 corner of the substrate is exposed;

18 performing a first rounding on the corner of the
19 substrate;

20 conformally forming a second insulating layer on the
21 first mask layer , the first insulating layer,
22 and the substrate;

23 forming an insulating plug on the second insulating
24 layer, such that the surface of the insulating
25 plug is substantially level with that of the
26 second insulating layer on the substrate;

27 removing the insulating plug, the second insulating
28 layer, and the first mask layer from the memory

29 cell array to expose the corner of the
30 substrate in the memory cell array region;
31 performing a second rounding process on the corner
32 of the substrate in the memory cell array
33 region.

1 14. The method as claimed in claim 13, wherein the
2 first mask layer comprises stacked silicon oxide and
3 silicon nitride layers.

1 15. The method as claimed in claim 13, wherein
2 removal of the edge of the first mask layer is performed
3 by anisotropic etching.

1 16. The method as claimed in claim 15, wherein an
2 etching solution comprising hydrogen fluoride (HF) and
3 ethylene glycol (EG) is employed in anisotropic etching.

1 17. The method as claimed in claim 13, wherein the
2 first rounding process comprises oxidizing the corner and
3 the sidewall of the first portion of the substrate to
4 form a sacrificial oxide layer and removing the
5 sacrificed oxide layer.

1 18. The method as claimed in claim 17, wherein
2 oxidization is performed by in-situ steam generation
3 (ISSG).

1 19. The method as claimed in claim 13, wherein the
2 second insulating layer comprises silicon nitride.

1 20. The method as claimed in claim 1, wherein the
2 insulating plug comprises silicon oxide formed by high
3 density plasma chemical vapor deposition (HDP CVD).

1 21. The method as claimed in claim 13, wherein the
2 second rounding process is performed by employing an
3 oxidation agent and a HF solution by turns.

1 22. The method as claimed in claim 21, wherein the
2 oxidation agent comprises $\text{H}_2\text{O}_2(\text{aq})$ and $\text{HNO}_3(\text{aq})$.

1 23. The method as claimed in claim 13, further
2 comprising forming transistors on the active area in the
3 memory cell array region and in the supporting region.